

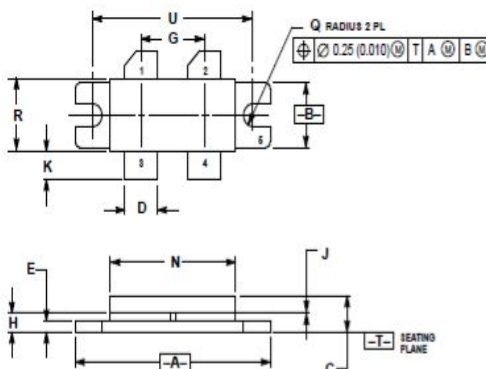
SILICON MOS N-CHANNEL RF POWER TRANSISTOR 150 W, up to 500 MHz, Enhancement Mode

MRF175GU

Designed primarily for wideband large-signal output and driver from 30–500 MHz.

Features:

- Performance at 400 MHz, 28 Vdc
- Power Gain: 10 dB Min
- Output Power: 150 W
- Efficiency: 55 % Min



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.330	1.560	33.78	39.62
B	0.370	0.410	9.40	10.41
C	0.190	0.230	4.83	5.84
D	0.215	0.235	5.47	5.96
E	0.050	0.070	1.27	1.77
G	0.450	0.460	10.92	11.68
H	0.100	0.112	2.59	2.84
J	0.034	0.036	0.86	0.91
K	0.185	0.210	4.69	5.33
N	0.945	0.975	24.05	24.72
Q	0.040	0.070	1.02	1.78
R	0.350	0.410	8.91	10.41
U	1.100 BSC		27.94 BSC	

STYLE 2:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

CASE 375-04

Absolute Maximum Ratings

Parameters	Sym	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V_{DC}
Drain Current-Continuous	I_D	8.0	A_{DC}
Gate-Source Voltage	V_{GS}	± 40	V_{DC}
Storage Temperature Range	T_{STG}	-65 tu +150	$^{\circ}C$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.44	$^{\circ}C/W$
Total Power Dissipation @ $T_C=25^{\circ}C$	P_D	400	W

Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage ($I_D=5.0$ mA, $V_{GS}=0$ V)	$V_{(BR)DSS}$	65	—	—	V_{DC}
Gate-Source Leakage Current ($V_{GS}=20$ V, $V_{DS}=0$ V) (1)	I_{GSS}	—	—	1.0	μA_{DC}
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28$ V, $V_{GS}=0$ V) (1)	I_{DSS}	—	—	2.5	mA_{DC}
Gate Threshold Voltage ($V_{DS} = 10$ V, $I_D = 25$ mA) (1)	$V_{GS(TH)}$	1	—	6	V_{DC}
Forward Transconductance ($V_{DS} = 10$ V, $I_D = 2.5$ A) (1)	G_{FS}	2	3	—	mhos
Input Capacitance ($V_{DS} = 28$ V, $V_{GS}=0$ V, $f = 1$ MHz) (1)	C_{ISS}	—	180	—	pF
Output Capacitance ($V_{DS} = 28$ V, $V_{GS}=0$ V, $f = 1$ MHz) (1)	C_{OSS}	—	200	—	pF
Reverse Transfer Capacitance ($V_{DS} = 28$ V, $V_{GS}=0$ V, $f = 1$ MHz) (1)	C_{RSS}	—	20	—	pF
Power Gain ($V_{DS} = 28$ V, $P_{OUT} = 150W$, $I_{DQ} = 200$ mA, $f = 400$ MHz)	G_p	10	12	—	dB
Drain Efficiency ($V_{DS} = 28$ V, $P_{OUT} = 150$ W, $I_{DQ} = 200$ mA, $f = 400$ MHz)	η_D	50	55	—	%

(1) Each transistor chip measured separately.

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Specification is subject to change without notice