

MRF157

SILICON MOS N-CHANNEL POWER TRANSISTOR 600 W, up to 80 MHz, Enhancement Mode

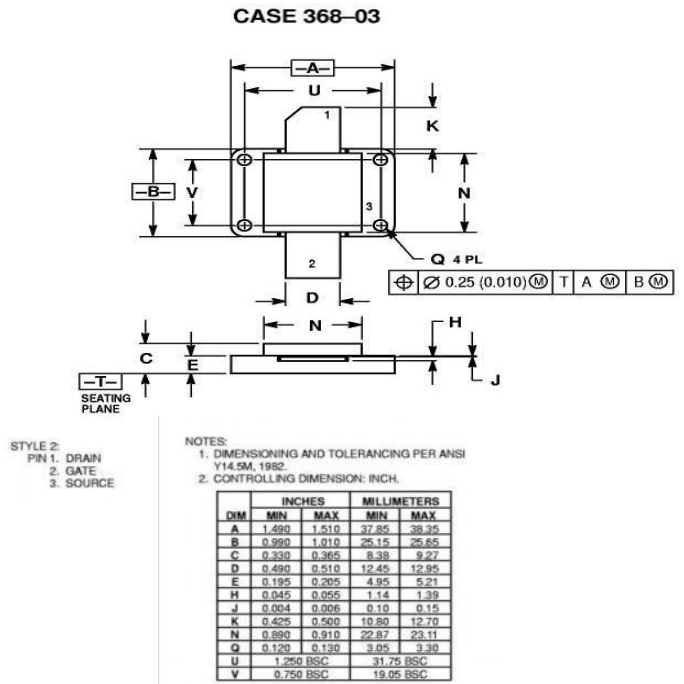
The silicon MOS transistor is designed for large-signal output stages to 80 MHz.

Features (at 30 MHz):

- Power Gain: 15 dB Min
- Output Power: 600 W
- Efficiency: 40% Min

Absolute Maximum Ratings

Parameters	Sym	Value	Unit
Drain-Source Voltage	V_{DSS}	125	V_{DC}
Drain Current-Continuous	I_D	60	A_{DC}
Gate-Source Voltage	V_{GS}	± 40	V_{DC}
Operation Junction Temperature	T_j	$-65 \div +200$	$^{\circ}C$
Storage Temperature Range	T_{STG}	$-65 \div +150$	$^{\circ}C$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.13	$^{\circ}C/W$
Total Power Dissipation	P_D	1350	W



Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage ($I_{DS} = 100 \text{ mA}$, $V_{GS} = 0 \text{ V}$)	$V_{(BR)DSS}$	125	—	—	V_{DC}
Gate-Source Leakage Current ($V_{GS}=20 \text{ V}$, $V_{DS}=0 \text{ V}$)	I_{GSS}	—	—	5	μA_{DC}
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 50 \text{ V}$, $V_{GS}=0 \text{ V}$)	I_{DSS}	—	—	20	mA_{DC}
Gate Threshold Voltage ($V_{DS} = 10 \text{ V}$, $I_D = 100 \text{ mA}$)	$V_{GS(TH)}$	1	3	5	V_{DC}
Forward Transconductance ($V_{DS} = 10 \text{ V}$, $I_D = 20 \text{ A}$)	G_{FS}	16	24	—	mhos
Input Capacitance ($V_{DS} = 50 \text{ V}$, $V_{GS}=0 \text{ V}$, $f = 1 \text{ MHz}$)	C_{ISS}	—	1800	—	pF
Output Capacitance ($V_{DS} = 50 \text{ V}$, $V_{GS}=0 \text{ V}$, $f = 1 \text{ MHz}$)	C_{OSS}	—	750	—	pF
Reverse Transfer Capacitance ($V_{DS} = 50 \text{ V}$, $V_{GS}=0 \text{ V}$, $f = 1 \text{ MHz}$)	C_{RSS}	—	75	—	pF
Power Gain ($V_{DS} = 50 \text{ V}$, $P_{OUT} = 600 \text{ W}$, $I_{DQ} = 800 \text{ mA}$, $f = 30 \text{ MHz}$)	G_p	15	20	—	dB
Drain Efficiency ($V_{DS} = 50 \text{ V}$, $P_{OUT} = 600 \text{ W}$, $I_{DQ} = 800 \text{ mA}$, $f = 30 \text{ MHz}$)	η_D	40	45	—	%

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Specification is subject to change without notice